What Is Claimed Is:

1. A memory circuit requiring refresh operations, comprising:

a memory core having memory cells;

a first circuit which receives a command supplied in synchronization with a clock signal, and which generates a first internal command internally;

a second circuit which generates a refresh command internally in a prescribed refresh cycle which is larger than the cycles of said clock signal; and

a memory control circuit which, according to said first internal command, executes corresponding control through clock-synchronous operations, and which, when said refresh command is issued, sequentially executes control corresponding to the refresh command and control corresponding to said first internal command through clock-asynchronous operations.

2. The memory circuit according to claim 1, wherein

said first circuit holds said first internal command corresponding to said supplied command, and

said memory control circuit generates internal command reception signals at the end of operation cycles, and receives said first internal command or refresh command in response to the internal command reception signal, and executes corresponding control.

3. The memory circuit according to claim 2, wherein said memory control circuit resets the command of said first circuit in response to reception of said first internal command, and resets the command of said second circuit in response to reception of said refresh command.

4. The memory circuit according to claim 2, wherein when said internal command reception signal occurs, if said first internal command or refresh command is generated, said memory control circuit executes control corresponding to the command, through clock-asynchronous operations; and,

when said internal command reception signal occurs, if said first internal command or refresh command is not generated, said memory control circuit waits for the command to be generated, and then executes control corresponding to the command which is generated later.

5. The memory circuit according to claims 1 through 4, further comprising a timer circuit; and, wherein said second circuit generates said refresh command based on refresh timing signals generated by the timer circuit.

6. An integrated circuit device, having a first circuit which receives commands supplied in synchronization with a clock signal and generates a first

internal command internally;

a second circuit which generates a second command internally, in a prescribed cycle larger than the cycles of said clock signal; and

an internal circuit which, according to said first internal command, executes corresponding control through clock-synchronous operations, and which, when said second command is issued, sequentially executes control corresponding to the second command and control corresponding to said first internal command through clock-asynchronous operations.

7. A memory circuit requiring refresh operations, comprising:

a memory core having memory cells;

a memory control circuit which, for M external operation cycles ($M \geq 2$), has N internal operation cycles, where N is greater than M ($M < N < 2M$); and,

a refresh command generation circuit which generates refresh commands; and, wherein

said N internal operation cycles include first internal operation cycle which executes external commands corresponding to said external operation cycles, and second internal operation cycle which executes said refresh commands.

8. The memory circuit according to claim 7, further

comprising an internal clock generation circuit which generates internal clock signals defining said internal operation cycles, according to an external clock signal which defines said external operation cycles; and, wherein said external commands are input in synchronization with said external clock signal, and said internal operation cycles are synchronized with said internal clock signal.

9. The memory circuit according to claim 8, wherein output of read data and input of write data are performed in synchronization with said external clock signal, and output of the read data from said memory core and input of write data to said memory core are performed in synchronization with said internal clock signal.

10. The memory circuit according to claim 8, wherein said internal clock generation circuit generates said N internal clock cycles for said M external clock cycles, and the N internal clock cycles include first internal clock cycle which control said first internal operation cycle, and second internal clock cycle which control said second internal operation cycle; and

said memory control circuit executes refresh operations in synchronization with said second internal clock cycles, in response to said refresh commands generated internally.

11. The memory circuit according to claim 8, wherein

said internal clock generation circuit generates said N internal clock cycles for said M external clock cycles, and the N internal clock cycles include first internal clock cycle which control said first internal operation cycle, and second internal clock cycle which control said second internal operation cycle;

said memory circuit has a refresh command generation circuit which, in response to refresh timer signals generated with a prescribed refresh cycle and to said second internal clock cycles, generates said refresh commands; and

said memory control circuit executes refresh operations according to said refresh commands.

12. The memory circuit according to claim 10, further having a power-down mode in which said external clock signal is not input, and wherein,

in the power-down mode, said memory control circuit executes said refresh operations in response to refresh timer signals generated in prescribed refresh cycles, regardless of said internal clock.

13. The memory circuit according to claim 11, further having a power-down mode in which said external clock signal is not input, and wherein

said refresh command generation circuit generates said refresh commands in response to said refresh timer signals, regardless of said second internal clock.

14. The memory circuit according to claim 7, 8 or 9, wherein

said memory control circuit performs a control corresponding to said refresh command at a plurality of second internal operation cycles.

15. The memory circuit according to claim 14, wherein,

within said plurality of second internal operation cycles, a prescribed number of consecutive first internal operation cycles are inserted.

16. The memory circuit according to claim 14, wherein,

within said plurality of second internal operation cycles, a prescribed number of consecutive first internal operation cycles are inserted, and said second internal operation cycles are shorter than said first internal operation cycles.

17. The memory circuit according to claim 14, wherein

said memory core has a data register which temporarily holds the data of memory cells being refreshed, and

said memory control circuit reads data in said

refreshed memory cells and holds the read data in said data register during the initial second internal operation cycle, and in the next second internal operation cycle rewrites to said refreshed memory cells the data held in said data register.

18. The memory circuit according to claim 17, wherein when the address in said initial second internal operation cycle and the address in the succeeding first internal operation cycle coincide, in the succeeding first internal operation cycle, reading or rewriting is performed according to the data held in said data register.

19. An integrated circuit device, operating in synchronization with a clock signal, comprising:

an internal circuit which, for M external operation cycles ($M \geq 2$), has N internal operation cycles, where N is greater than M ($M < N < 2M$), and wherein

said N internal operation cycles have first internal operation cycles which execute external commands corresponding to said external operation cycles, and second internal operation cycles which execute internal commands.

20. The integrated circuit device according to claim 19, further comprising:

an internal clock generation circuit which generates

an internal clock signal defining said internal operation cycles, according to an external clock signal which defines said external operation cycles; and wherein

said external commands are input in synchronization with said external clock signal, and said internal operation cycles are synchronized with said internal clock signal.

21. A memory circuit requiring refresh operations, comprising:

a memory core having memory cells;

a memory control circuit which, for M external operation cycles ($M \geq 2$), has N internal operation cycles, where N is greater than M ($M < N < 2M$); and

a refresh command generation circuit which generates refresh commands; and wherein

said N internal operation cycles includes first internal operation cycles which execute external commands corresponding to said external operation cycles, and second internal operation cycles which execute said refresh commands, and

said refresh command generation circuit generates said refresh commands according to a reception of said external command.

22. The memory circuit according to claim 21, wherein the frequency of said external clock signal is higher than

the frequency of said external operation cycles;

further comprising an internal clock generation circuit which generates an internal clock signal defining said internal operation cycles according to the external clock signal; and,

said external commands are supplied according to a cycle which is equal to or greater than said external operation cycle, and are input in synchronization with said external clock signal.

23. The memory circuit according to claim 22, wherein said refresh command generation circuit permits the generation of said refresh commands according to the combination of external commands, which are input in synchronization with a prescribed number of said external clock cycles.

24. The memory circuit according to claim 22, wherein said refresh command generation circuit permits the generation of said refresh commands when said external commands are not input in synchronization with any of the external clock cycles among a prescribed number of said consecutive external clock cycles.

25. The memory circuit according to claim 22, wherein in cases where the frequency of said external commands is L times the frequency of said external

operation cycles, said refresh command generation circuit permits the generation of said refresh commands when said external commands are not input in synchronization with any of (L-1) external clock cycles among said L consecutive external clock cycles, and within said M external operation cycles, combinations of said (L-1) external clock cycles are circulated.

26. The memory circuit according to claim 22, wherein in cases where the frequency of said external commands is L times the frequency of said external operation cycles, further comprising:

an internal command register which holds said external commands in the most recent L external clock cycles, and generates corresponding internal commands according to the held external commands; and wherein

in prescribed cycles among said N internal operation cycles, said internal command register ignores the held external commands in some cycles among said L held external commands, and generates said internal commands.

27. The memory circuit according to claim 26, wherein said refresh command generation circuit permits generation of said refresh commands according to internal commands generated by said internal command register.

28. The memory circuit according to claim 26, wherein

said refresh command generation circuit permits the generation of said refresh commands when there exist no internal commands generated by said internal command register.

29. The memory circuit according to claims 23 through 28, wherein

said refresh command generation circuit generates said refresh commands during a state of permission of said refresh command generation, in response to generation of refresh timer signals generated with prescribed timing.

30. A memory circuit requiring refresh operations, comprising:

a memory core having memory cells;

a first circuit which receives a command supplied in synchronization with an external clock signal, and which generates a first internal command internally;

a second circuit which generates a refresh command internally in a prescribed refresh cycle which is larger than the cycle of said external clock signal; and

a memory control circuit which includes a first internal operation cycle and a second internal operation cycle shorter than said first internal operation cycle, executes control corresponding to said first internal command according to the first internal operation cycle, and when said refresh command is issued, sequentially

executes a control corresponding to the refresh command and a control corresponding to said first internal command according to the second internal operation cycle.

31. The memory circuit according to the claim 30, wherein

the memory control circuit executes the corresponding control according to the first internal operation cycle while a finish timing of the internal operation is faster than a generation timing of the first internal command or the refresh command, whereas, executes the corresponding control according to the second internal operation cycle while the generation timing of the first internal command or the refresh command is faster than the finish timing of the internal operation.

32. An integrated circuit device operating in synchronous with a clock signal, comprising:

a first circuit which generates a first internal command internally according to a command externally received;

a second circuit which generates a second internal command internally, in a prescribed cycle larger than the cycles of an external command cycle; and

an internal circuit which includes a first internal operation cycle according to which an internal operation is executed in synchronous with the external operation

cycle, and a second internal operation cycle according to which the internal operation is executed in a shorter cycle than the first internal operation cycle;

wherein the internal circuit executes an operation corresponding to the first internal command according to the first internal operation cycle in a normal state, and executes an operation corresponding to the first and second internal commands according to the second operation cycle during a prescribed period after generation of the second internal command.

33. A memory circuit requiring refresh operations, comprising:

a memory core having memory cells;

a first circuit which receives external commands supplied with an interval equal to or longer than a minimum external command cycle, and which generates a first internal command internally;

a second circuit which generates a refresh command internally in a prescribed refresh cycle which is larger than the minimum external command cycle; and

a memory control circuit which executes internal operation corresponding to the first internal command according to an internal operation cycle shorter than the minimum external command cycle;

wherein the memory control circuit executes an internal operation corresponding to said first internal

command in response to a timing of the external command while a finish timing of the internal operation cycle is faster than the timing of the external command, and when said refresh command is issued, sequentially executes control corresponding to the refresh command and control corresponding to said first internal command according to the internal operation cycle.

34. The memory circuit according to the claim 33, wherein when the internal operation is finished, the memory control circuit receives the first internal command generated by the first circuit or the refresh command generated by the second circuit, and executes the corresponding internal operation.